# DESIGN OF CLOCK RECOVERY MMIC USING LARGE-SIGNAL COMPUTER-AIDED ANALYSIS

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## ABSTRACT

Next generation of Gb/s local area distribution networks employed as optical interconnects are designed using OEIC technology for low power consumption, high reliability, and low cost. A hybrid optoelectronic integrated circuit (OEIC) integrated with MMIC circuits is described in this paper as a first step toward full monolithic integration. Si MMIC foundry services from Bipolarics was selected to design an optical receiver with an injection locked phase lock loop (ILPLL) clock recovery circuit at 1.25 Gb/s. The simulation has indicated that the input noise equivalent voltage density of the receiver is lower than 0.6 nV/$\sqrt{Hz}$ for frequency up to 1 GHz. The simulated minimum received optical power to extract the clock signal is -30 dBm. The output clock signal of this clock recovery circuit is about 400 $mV_{p-p}$. Simulated power consumption is 630 mW for the optical receiver and the ILPLL clock recovery circuit.

## I. INTRODUCTION

The future local area distribution systems and military distribution systems will require data transfers between various signal processors, sensors, and video distribution nodes at rates well above Gb/s. One of the limiting factors in design of the optical transceivers is their high prime power requirements, particularly in the clock recovery circuit. in addition to the low power consumption design requirements, the clock recovery circuit should satisfy the high reliability, small size, and light weight requirements.

The demand for low power consumption, high reliability, and small size clock recovery and decision circuits has pushed the technology towards hybrid optoelectronics integrated circuits (OEIC's) realization. Rein [1] has demonstrated a clock recovery circuit using XOR up to 3.4Gb/s, whereas Ross et al [2] demonstrated a frequency multiplier and SAW filter to extract the clock signal. Another technique commonly employed for clock extraction is based on the PLL approach [3-5]. For example, Buchward et al [3] demonstrated a 6 GHz PLL clock recovery circuit using HBT for 10Gb/s SONET applications. However, most of the approaches reported for MMIC circuit designs consume high prime power.

An alternative method to the conventional clock recovery circuit is Injection Locked Phase lock Loop (ILPLL), which was demonstrated at 1.25Gb/s using a hybrid MIC circuit [6]. This approach consumes much lower prime power than PLL and provides a larger tracking range, a shorter pull-in time, and much cleaner close-in to carrier phase noise. In order to reach the system requirements a fully integrated optical receiver, clock recovery and decision circuit is proposed. However, this paper addresses issues associated with monolithic integration and realization of a hybrid version of the optical receiver with the ILPLL.

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## II. DESIGN PHILOSOPHY

For design of the MMIC's, we have decided to use the Si based foundry services, from Bipolarics Inc., due to its low-cost and excellent thermal conductivity. The 0.5 micron SiMMIC process of Bipolarics provides option of BJT transistors with $I_c$ of 10mA to 40mA with emitter size of 0.6x0.2 $\mu m^2$. The BTA24 transistor array have a typical gain bandwidth product of $f_T$=10 GHz with breakdown voltage $BV_{ceo}$=12V. Resistors are fabricated using a thin film tantalum nitride layer deposited over thick oxide to give low leakage and good absolute tolerance. Three values of resistivity are possible: 100Ω/square, 500Ω/square, and 1000Ω/square. Capacitors are manufactured using metal-oxide, and a range of 0.03 to 0.15 fF/$\mu m^2$ is achievable by adjusting the oxide thickness. A hybrid design is pursued for the clock recovery circuit, since realization of this circuit at frequencies of 1.25GHz requires large value inductors and capacitors, which occupy a lot of space in MMIC.

In the design of silicon MMIC's, linear performance of the designed circuit was first simulated using the small-signal model of BJT, followed by nonlinear performance evaluation and optimization using the large-signal model. Time-domain large-signal analysis using MWSPICE is a very useful tool to simulate performance of the voltage



CH3577-4/95/0000-1181$01.00 © 1995 IEEE

controlled oscillator and phase detector of the clock recovery circuit. Performance of the optical receiver was evaluated using the custom designed microwave photonics CAD. A meaningful analysis result is contingent on the accuracy of the BJT's SPICE model. Bipolarics, Inc. has provided the BJT Gummel-Poon model in SPICE. In addition to requiring the accurate active device model, the parasitics effects are taken into account to consider the effects of chip packaging and hybrid integration of MMICs. SIOC 8 plastic packages are selected for integration of 40x40 $mil^2$ MMIC chips with the passive components, such as 35x35 $mil^2$ chip capacitors. These packaged MMICs are mounted on a low temperature confined ceramic using the surface mount technology.

## III. DESIGN OF THE CLOCK RECOVERY CIRCUIT

The block diagram of the designed hybrid OEIC clock recovery circuit is shown in Fig. 1. Based on this circuit topology, the designed MMIC circuits are realized for optical fiber communication systems at 4B5B NRZ data rates up to 1.25 Gb/s. The optical receiver is a hybrid OEIC, which includes a pin photodiode and a trans-impedance MMIC amplifier. The output of the optical trans-impedance amplifier is inputted to the clock recovery and also as the data signal to the decision circuit. The clock extraction at 1.25GHz is based on filtering the 625MHz spectra line of the 4B5B NRZ data at 1.25Gb/s using an external bandpass filter, followed by the ILPLL at 625MHz and a MMIC frequency doubler, as represented in block diagrams in Fig. 1. Two other tank circuits are realized outside the MMIC's to avoid low Q factor and the large space required. The OMN is an idler circuit at 1.25GHz to recover the 1.25 GHz output of the frequency doubler. Since varactor diodes are not available from Bipolarics foundry, the oscillator feedback is also built outside the MMIC gain stage. In fact, because capacitance of the varactor diode and the inductor in the feedback path form the resonant frequency of the oscillator, a higher $Q_{ex}$ is obtained for this oscillator. The DC signal generated by the phase detector, amplified by the loop filter, changes dc bias of the varactor diode. This closed loop circuit phase locks the oscillator for any frequency drift of the free-running oscillator within the pull-in range of the ILPLL. The design and simulated performance for each individual MMIC are presented next.

i) Trans-impedance Amplifier Design: The schematic of the trans-impedance amplifier MMIC is shown in Fig. 2. The first step in the design of optical receiver is to choose a suitable photodetector. A BT&D (model:PDH0004) InGaAs pin photodiode is chosen due to its low dark current and high responsivity at 1300nm. Typically, the photodetector has 0.9 mA/mW optical responsivity and 5nA electrical dark current. The equivalent circuit model of this photodiode is extracted and used in design of the optical receiver. The photodiode output is amplified by a cascaded two stage amplifiers with first two transistors comprise the feedback pair [7]. The first transistor Q1 is in a common emitter configuration followed by an emitter follower Q2 with trans-impedance from the emitter of the second transistor to the base of the first transistor. The purpose of using the emitter follower Q2 here is to maximize the loop gain and reduce capacitive loading at the high impedance collector of Q1. The third stage is a common emitter transistor with feedback to provide the required flat gain and filter the unwanted signal. A power consumption of 137mW is predicted for this circuit.

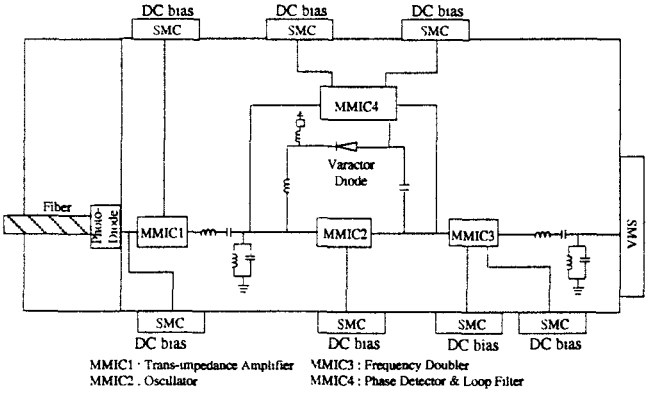


Fig. 1 Block diagram layout presentation of the clock recovery MMIC's module.

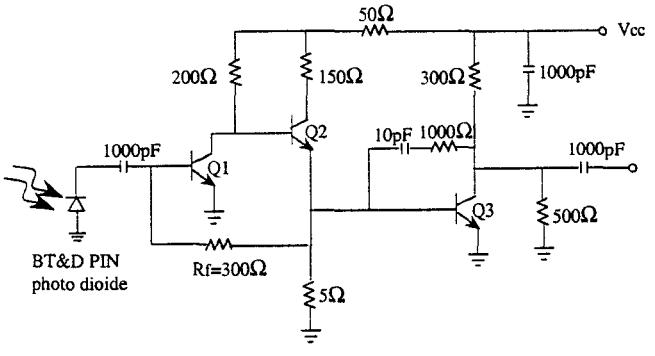


Fig. 2 Schematic circuit diagram of the trans-impedance amplifier with its typical values.

ii) Voltage Controlled Oscillator Design: The oscillator contains an active device $Q_1$ and the active bias circuitry as shown in Fig. 3. The capacitors $C_1$ and $C_2$ are used

as DC blocks while the Resistors $R_b$ and $R_c$ are the bias resistors and transistors $Q_2$ and $Q_3$ are used for active bias components. The RF choke $L_1$ and by-pass capacitor $C_3$ are realized outside the MMIC. As shown in Fig. 2, the feedback path is also built outside the MMIC since the length of the feedback path is too long to be fabricated inside the MMIC. Due to their large size, the varactor diode and inductor, which form the resonant circuit of the oscillator, are also realized outside the MMIC. A silicon hyper-abrupt junction diode from Frequency Sources (model no: GC1510) was selected because of its high sensitivity (i.e.; a tuning range of ≈ 47 MHz for the at 625MHz oscillator). A power consumption of 65mW is predicted for this VCO.

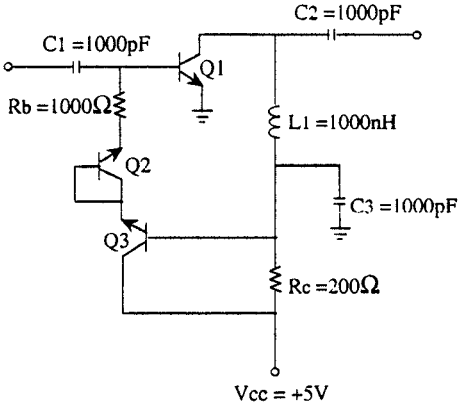


Fig. 3 Schematic of the proposed voltage controlled oscillator.

iii) Phase Detector With Loop Filter: The circuit topology we used for the phase detector is the Gilbert multiplier [8, 9] as shown in Fig. 4. The Gilbert multiplier is a variable transconductance multiplier realized by a pair of differential amplifier. The output voltage of the differential amplifier depends on the transconductance $g_m$ of the BJTs. The transconductance of the BJTs, $g_m$, depends on the magnitude of $I_o$, where $I_o$ is a constant current source provided by the transistor $Q_7$. The RF signal is provided to a differential pair and multiplied by $\pm V(f_{LO})$ to provide a double-balanced mixer characteristics.

A differential loop filter was realized using RC low pass filter. The high frequency components from the mixer is filtered out and DC or low frequency components are passed through. The output signal from the loop filter is amplified by a single stage amplifier and inputted to the varactor diode to adjust the oscillating frequency of the oscillator. The predicted power consumption of this phase detector 284mW.

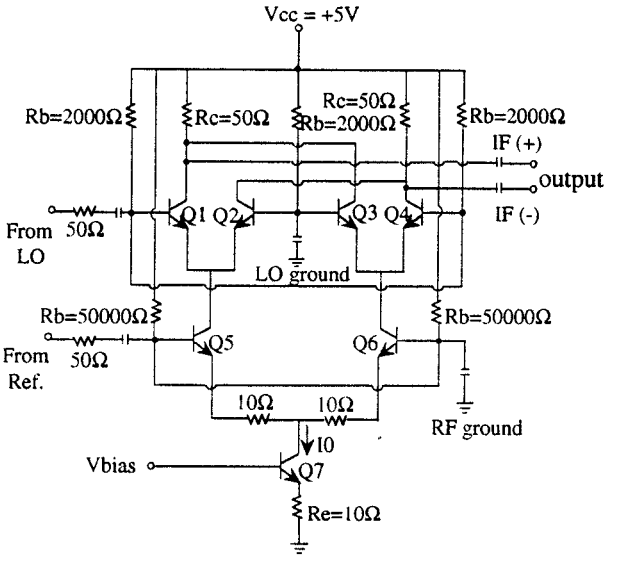


Fig.4 Schematic of the phase detector using Gilbert multiplier.

iv) Frequency Doubler Design: The circuit topology for the frequency doubler is shown in Fig. 5. It consists of an input buffer stage and a frequency doubler. The input buffer stage added after the output of the oscillator is used to reduce pulling effect due to the load impedance change. In order to achieve high nonlinearity of the frequency doubler, the BJT is operated in class B, resulting in a low power consumption. A tank circuit, OMN, is used to reflect any signal other than 1.25 GHz clock signal back to the frequency doubler. This tank circuit, composed of lumped inductor and capacitor, is built outside the MMIC. The predicted consumed power of this doubler is 144mW.

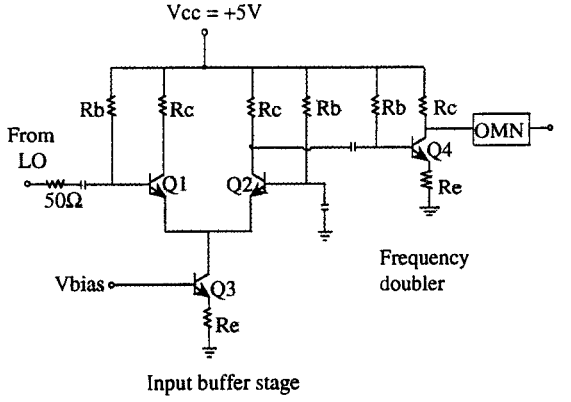


Fig. 5 Schematic of the frequency doubler.

## IV. SIMULATED PERFORMANCE OF THE CLOCK RECOVERY CIRCUIT

The performance of the clock recovery circuit was predicted using EESOF/MWSPICE. A 0dBm rf signal at 625MHz is inputted to a LED based optical transmitter model as an equivalent ECL-compatible 4B5B NRZ data pattern. A voltage controlled current source (VCCS) with a transconductance of 1mS, equivalent to the transducer gain of the fiberoptic link realized using the Lyetl LED and BT&D pin photodiode [6]. This loss includes the optoelectronic losses due to LED and detector conversion efficiency as well as the connector and fiber losses.

A short transient stimulus is applied to the active device of the oscillator to trigger the oscillation and have it phase and frequency locked to the 625MHz reference extracted from the 1.25Gb/s NRZ data. The output of the time-domain analysis was Fourier transformed to get the output power spectrum. The Fourier transformed of the recovered clock at the output of the frequency doubler is shown in Fig. 6. As shown, the frequency doubler has strongest component at 1.25 GHz; the recovered clock has a peak-to-peak output voltage about 0.4V, which corresponds to a 3 dBm power output.

Both frequency and amplitude sensitivity of this clock recovery circuit was also simulated. The tracking range of this clock recovery oscillator for 0dBm input power to VCO is 625±15 MHz. The simulated minimum input power required of this clock recovery circuit to acquire phase locking is calculated to be -30 dBm. The overall power consumption of this optical receiver/clock recovery circuit is calculated to be about 630mW, which is a very low figure compared to other reported work. This circuit is layed-out and is in process to be fabricated.

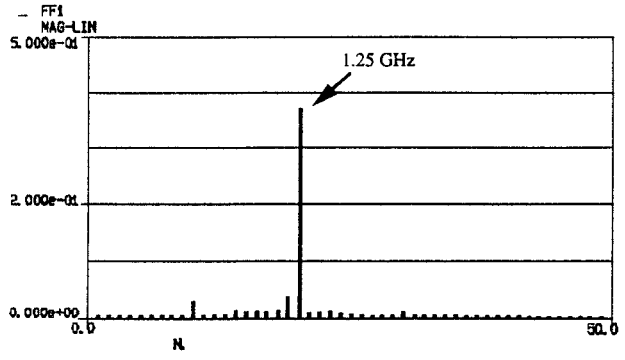


Fig. 6 Fourier transform at the output of clock recovery circuit at 1.25 GHz.

## V. CONCLUSION

This paper presented design and simulation of a low power consuming hybrid MMIC optical receiver and ILPLL clock recovery circuit. The total power consumption of this module is calculated to be about 630mW. This is a very low figure and is very attractive for local area distribution networks and military data distribution systems.

## ACKNOWLEDGEMENTS

This work is supported by NAWC, Aircraft Division, Warminster, PA. Valuable comments of Drs. W. Rosen (NAWC), C. Leung (Bipolarics), and X. Zhang (Drexel) are appreciated.

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